REMARKS

Claims 1 to 17 are currently pending in the present application. Claims 1, 4 to 11, 13 to 15 and 17 stand rejected. Claims 2, 3, 12 and 16 are objected to. Claims 1, 2, 11 and 16 are amended. Claim 12 is cancelled. The amendments are supported by the application as originally filed. Therefore no new matter has been added by the amendments. Reconsideration of the present application, as amended, is respectfully requested.

Claims 1, 4 to 11, 13 to 15 and 17 stand rejected by the Action under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,529,421 to Marr et al. (hereinafter "Marr") in view of U.S. Patent No. 5,223,753 to Lee et al. (hereinafter "Lee") and U.S. Patent No. 5,087,830 to Cave et al. (hereinafter "Cave").

Independent claim 1 is amended in order to more clearly define the present claimed invention over the cited references. Amended claim 1 claims a control unit controlling a threshold voltage of a circuit unit having a plurality of transistor devices, comprising a reference circuit; a measuring unit measuring a threshold voltage of at least one sensing transistor of the circuit unit and measuring a reference threshold voltage of at least one reference transistor of the reference circuit; a differential voltage generator generating a differential voltage from outputs of the measuring unit, the voltage generator comprising an averaging unit, a comparing unit and an amplifier, and a bulk connection of the transistor devices in the circuit unit to which the differential voltage is fed as a biasing voltage.

Neither Marr nor Lee nor Cave, taken either alone or in combination, teaches the invention as set forth in claim 1, as amended. Specifically, claim 1 now clearly claims a differential voltage generator generating a differential voltage from outputs of the measuring unit, the voltage generator comprising an averaging unit, a comparing unit and an amplifier.

Marr is directed to a transistor body bias generator having a temperature-compensated threshold voltage. An increase in temperature in the circuit significantly increases the leakage current and decreases the V_{TN} in a LL4TCMOS SRAM cell, which causes significant data retention problems for the cell. As conceded by the Action, Marr fails to disclose the details of a differential voltage generator, as is now clearly claimed in claim 1.

Lee and Cave also fail to disclose a differential voltage generator generating a differential voltage from outputs of the measuring unit, the voltage generator comprising an averaging unit, a comparing unit and an amplifier, as is now clearly claimed in claim 1. Lee is directed to an operational amplifier or a comparator, and more particularly to a circuit which can improve the slew rate (the response speed of an output signal as a function of an input signal) of the operational amplifier having a capacitive load at an output terminal. Cave is directed to a start circuit for a bandgap reference cell using CMOS transistors and more particularly to apparatus and method for starting a bandgap reference cell by introducing an offset voltage. As conceded by the Action, both Lee and Cave fail to teach or suggest that the differential voltage generator comprises: an averaging unit forming at least one average threshold value of at least one measured transistor voltage of the circuit unit; a comparing unit comparing at least one average threshold voltage value of the circuit unit with at least one measured transistor threshold voltage of the reference circuit and creating at least one different voltage value indicating the difference between at least one average threshold voltage value of the circuit unit and at least one transistor threshold voltage of the reference circuit; an amplifier unit amplifying at least one difference voltage value of the comparing unit and creating at least one amplified difference voltage value.

The Action suggests that it would have been obvious to use Lee's comparator and Cave's bandgap circuit for the purpose of saving power in Marr's circuit. Applicants respectfully traverse this suggestion as evidenced by the fact that Marr actually teaches

away from the suggested combination. A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). Marr's solution for current leakage in a transistor body bias generator is to control the temperature-compensated threshold voltage. Marr teaches that increases in temperature in a circuit significantly increase the leakage current and decrease the V_{TN} in a cell, causing significant data retention problems for the cell.

In contrast, the subject application is directed to a control unit controlling a threshold voltage of a circuit unit having a plurality of transistor devices. The subject application teaches that threshold voltage variability can have a deleterious impact on circuit performance. Namely, it has an adverse impact on power consumption and cell delay. With technology scaling into the deep-submicron domain, statistical variations of threshold voltage within a chip are more obvious. Equally important are the variations that arise due to the scaling of the power supply and corresponding voltage bounce. Thus, it is an object of the subject application to provide a control unit controlling a threshold voltage of a circuit unit, an integrated circuit (IC) device comprising a circuit unit and a control unit controlling a threshold voltage of a circuit unit and a method for controlling a threshold voltage of a circuit unit which are able to cope with differences in the threshold voltages of a plurality of transistors of a circuit unit whose differences are caused for example by fabrication mismatch, temperature gradients, circuit noise, etc. The subject application enables the control of fabrication mismatch by e.g. noise, V_t mismatch. Such control is useful for every IC production particularly for deep submicron IC's which are sensitive to such fabrication mismatches. Accordingly, claim 1 of the subject application is directed to a means for controlling threshold voltage variability, which can have a deleterious impact on circuit performance such as power consumption and cell delay. Claim 1 claims a control unit for controlling a threshold voltage of a circuit unit having a plurality of transistor devices comprising a differential voltage

generator generating a differential voltage from outputs of the measuring unit, the voltage generator comprising an averaging unit, a comparing unit and an amplifier, and a bulk connection of the transistor devices in the circuit unit to which the differential voltage is fed as a biasing voltage.

Moreover, to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). As discussed above, the cited combination fails to suggest all elements of claim 1, as amended.

In view of the foregoing, independent claim 1 is patentable over of Marr, Lee and Cave when taken either singly under 35 U.S.C. § 102 or in combination under 35 U.S.C. § 103(a). Therefore, claim 1 is patentable over all of the references of record under 35 U.S.C. § 102 as well as 35 U.S.C. § 103(a). Accordingly, the rejections under 35 U.S.C. § 103(a) of claim 1 should be withdrawn and claim 1 should be allowed.

Claims 2 to 10 are either directly or indirectly dependent on claim 1 and are patentable over the references of record in view of their dependence on claim 1 and because the references of record do not disclose, teach or suggest each of the limitations set forth in claims 2 to 10.

Claim 11 has been amended to claim a method for controlling of at least one threshold voltage of transistors in a circuit unit; providing at least one reference transistor and measuring a threshold voltage of the at least one reference transistor; generating a differential voltage from outputs of the measuring unit comprising the steps of: forming at least one average threshold voltage value of at least one measured transistor threshold voltage of the circuit unit; comparing at least one average threshold voltage value of the circuit unit with at least one measured transistor threshold voltage of the reference circuit and creating at least one difference voltage representing the difference between at least

one average threshold voltage value of the circuit unit and at least one transistor threshold voltage of at least one reference transistor; and amplifying the at least one difference voltage of the comparing unit and creating at least one amplified difference voltage, and feeding the differential voltage as a biasing voltage to a bulk connection of the transistor devices in the circuit unit.

Neither Marr nor Lee nor Cave, taken either alone or in combination, teaches the invention as set forth in claim 11, as amended, for the reasons discussed with respect to claim 1. Thus, independent claim 11 is patentable over of Marr, Lee and Cave when taken either singly under 35 U.S.C. § 102 or in combination under 35 U.S.C. § 103(a). Therefore, claim 11 is patentable over all of the references of record under 35 U.S.C. § 102 as well as 35 U.S.C. § 103(a). Accordingly, the rejections under 35 U.S.C. § 103(a) of claim 11 should be withdrawn and claim 11 should be allowed.

Claims 13 to 17 are either directly or indirectly dependent on claim 11 and are patentable over the references of record in view of their dependence on claim 11 and because the references of record do not disclose, teach or suggest each of the limitations set forth in claims 13 to 17.

Conclusion

In view of the foregoing, Applicants respectfully submit that the specification, the drawings and all claims presented in this application are currently in condition for allowance. Accordingly, Applicants respectfully request favorable consideration and that this application be passed to allowance.

Should any changes to the claims and/or specification be deemed necessary to place the application in condition for allowance, the Examiner is respectfully requested to contact the undersigned to discuss the same.

Applicants' representative believes that this response is being filed in a timely manner. In the event that any extension and/or fee is required for the entry of this amendment the Commissioner is hereby authorized to charge said fee to Deposit Account No. 14-1270. An early and favorable action on the merits is earnestly solicited.

If the Examiner should have any questions concerning this communication or feels that an interview would be helpful, the Examiner is requested to call David Barnes, Esq., Intellectual Property Counsel, Philips North America Corporation at the number below.

Respectfully submitted,

Reg. No. 45,667

for Dave Barns, Esq.

Philips Electronics North America Corporation 345 Scarborough Road Briarcliff Manor, New York 10510

Phone: 914-333-9693 Fax: 914-332-0615